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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,705	12/28/2001	Myoung Goo Lee	0630-1296P	3917

2292 7590 08/21/2003

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EXAMINER
KITOV, ZEEV

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,705	LEE ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8, 10 - 14, 16* is/are rejected.

7)☒ Claim(s) *9 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Oath or Declaration Defective

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because it does not identify the citizenship of each inventor.

2. Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. However, according to Fig. 3, the base-emitter junction of a bipolar transistor B1 as well as a gate-source of NMOS transistor is short-circuited and therefore none of the transistors can be controlled by external signal, such as a current flow through the diodes. Therefore, the Fig. 3 requires correction. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Avery et al. (US 6,501,632).

Regarding Claim 1, Avery et al. disclose all the elements of the claim including an electrostatic discharge (ESD) protection circuit having an NMOS transistor connected between an input/output pad and a ground (element NMOS in Fig. 3), the NMOS transistor having a parasitic bipolar transistor (element NPN in Fig. 3); and at least one diode connected between the input/output pad and the NMOS transistor (element Z3 in Fig. 3, col. 2, lines 44 – 67, col. 3, lines 1 - 10).

Regarding Claim 3, Avery et al. disclose the diode as a PN diode (element Z3 in Fig. 3).

4. Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

a) Claims 2, 4, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avery et al. (US 6,501,632) in a view of Menon et al. (US 4,795,918). As was stated above, Avery et al. disclose all the elements of Claim 1. However, regarding Claim 2, they do not disclose a diode being connected in specific polarity, namely by its cathode to the base of the transistor. Menon et al. disclose a bipolar transistor having a diode connected to the transistor base by its output terminal (cathode) (elements 40 in Fig. 2, col. 3, lines 28 – 38). Both patents have the same problem solving area, namely providing the bipolar transistor with bias through forward biased diode. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Avery et al. solution and replacing the zener diode by the forward biased diodes according to Menon et al., because it is well known in the art, that the zener diode and a group of forward biased diodes are interchangeable and that selection of particular solution is up to designer according to his secondary considerations, such as for example, thermal stability. The forward biased diodes are widely used in the design of band-gap reference voltage sources.

Regarding Claim 4, Mennon et al. disclose at least one diode as a plurality of PN diodes. The motivation for modification of the primary source is the same as above.

Regarding Claim 5, Avery et al. disclose that the zener diode is selected so as to stop a current flow through the at least one diode during a normal operation of a chip

(col. 3, lines 20 – 5). Accordingly, the amount of forward biased diodes in the Avery et al. structure modified according to Menon et al. is selected the same way.

Regarding Claim 6, Menon et al. disclose the plurality of N diodes as connected in series to each other in a forward direction (elements 40 in Fig. 2, col. 3, lines 28 – 38). The motivation for modification of the primary source is the same as above.

Regarding Claim 7, Avery et al. disclose connection of a threshold element (the zener diode Z3) connected between the input/output pad and a high voltage p-well (element HVPW in Fig. 4), which is an extension of a p-substrate of an NMOS transistor. As to connection of diodes, Menon et al. disclose a structure, wherein p+ and n+ junctions of a first diode of the plurality of N diodes are connected to the input/output pad and a p+ junction of a second diode of the plurality of N diodes, respectively, the second diode through the N-1 diode of the plurality of N diodes are connected such that an n+ junction of each of the second diode through the N-1 diode is connected to the p+ junction of a subsequent diode, and an n+ junction of an N diode is connected to the transistor. The motivation for modification of the primary source is the same as above.

Regarding Claim 8, Avery et al. disclose an electrostatic discharge protection circuit having an input/output pad (element 302 in Fig. 3) and the NMOS transistor (element NMOS in Fig. 3) connected between the input/output pad and having a parasitic bipolar transistor (element NPN in Fig. 3) connected to the zener diode (element Z3 in Fig. 3). Avery et al. further disclose the zener diode Z3 connected between the input/output pad and a high voltage p-well (element HVPW in Fig. 4), which is an extension of a p-substrate of an NMOS transistor; and the NMOS transistor as

being connected between the input/output pad and having a parasitic bipolar transistor connected to the zener diode Z3. As to replacement of the zener diode by the plurality of N diodes, Menon et al disclose it. The replacement was discussed above.

Regarding Claim 10, Menon et al. disclose the plurality of PN diodes (elements 40 in Fig. 3). The motivation for modification of the primary source is the same as above.

Regarding Claim 11, Avery et al. disclose that the zener diode is selected so as to stop a current flow through the at least one diode during a normal operation of a chip (col. 3, lines 20 – 5). Accordingly, the amount of forward biased diodes in the Avery et al. structure modified according to Menon et al. is selected the same way.

Regarding Claim 12, Avery et al. disclose connection of a threshold element (the zener diode Z3) connected between the input/output pad and a high voltage p-well (element HVPW in Fig. 4), which is an extension of a p-substrate of an NMOS transistor. As to connection of diodes, Menon et al. disclose a structure, wherein p+ and n+ junctions of a first diode of the plurality of N diodes are connected to the input/output pad and a p+ junction of a second diode of the plurality of N diodes, respectively, the second diode through the N-1 diode of the plurality of N diodes are connected such that an n+ junction of each of the second diode through the N-1 diode is connected to the p+ junction of a subsequent diode, and an n+ junction of an N diode is connected to the transistor. The motivation for modification of the primary source is the same as above.

Regarding Claim 13, Avery et al. disclose the circuit, wherein the anode of the zener diode is connected to the base of the parasitic bipolar transistor (elements Z3 and

NPN in Fig. 3). As was explained above, the Menon et al. reference provides a solution for modification of the Avery et al. circuit replacing the zener diode by the plurality of N diodes connected to the base of the parasitic bipolar transistor. The motivation for modification of the primary source is the same as above.

Regarding Claim 16, Menon et al. discloses the diodes as PN diodes. The motivation for modification of the primary source is the same as above.

b) Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Avery et al in a view of Menon et al. and further in a view of Duvvury et al. (5,814,865). Regarding Claim 14, Avery et al. disclose an electrostatic discharge (ESD) protection circuit having an input/output pad (element 302 in Fig. 3), and the (zener) diode connected between the input/output pad and a high voltage p-well (element HVPW in Fig. 3), which is an extension of the substrate of an NMOS transistor, and the NMOS transistor connected between the input/output pad and having a parasitic bipolar transistor connected to the (zener) diode. Menon et al. disclose the plurality of N diodes. However, they neither disclose the plurality of N diodes connected to the base of the bipolar transistor, nor at least two diodes connected in parallel. The plurality of N diodes connected to the base of the bipolar transistor as disclosed by Menon et al. and appropriate motivation for modification of the primary reference was discussed above. As to diodes connected in parallel, these elements are disclosed by Duvvuri et al. (US 5,814,865) (Fig. 2 and 2a, col. 4, lines 9 –37). Both patents have the same problem solving area, namely ESD protection of electronic circuits. Therefore, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Avery et al. circuit according to the Duvvury et al., because as Duvvury et al. state (col. 4, lines 9 –37), since the two diodes are in parallel, they, as a pair, will have a lower resistance.

5. Allowable Subject Matter

Claims 9 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that they recite the substrate as being connected to a ground. This limitation was not found in the collected prior art of the record.

6. Conclusion

The prior art made of record not relied upon is considered pertinent to applicant's disclosure: US 6,292,343, US 6,529,359, US 6,437,407, US 6,399,990.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone numbers for organization where this application or proceedings is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
08/07/2003

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